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Response Under 37 CFR 1.116
Expedited Procedure
Examining Group 2814

Surles 12/4/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application of

Applicant	:	Joseph M. Brand
Serial No.	:	09/335,618
Filed	:	June 18, 1999
Title	:	ENCAPSULANT LOCK FEATURE
Docket No.	:	MIO 0051 PA
Examiner	:	Alonzo Chambliss
Art Unit	:	2814

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF FACSIMILE
I hereby certify that this correspondence is being facsimiled to (703) 308-7722, on October 15, 2001.

Attorney 42,695 Reg. No.

Do not enter this amendment. AC 10/26/01

Sir:

AMENDMENT AFTER FINAL REJECTION

This paper is being filed in response to the office action made final and dated July 24, 2001 in the identified application, having a reply due date of October 24, 2001. Reconsideration and reexamination are respectfully requested in light of the amendments and remarks below.

In the Claims

The entire set of presently pending claims has been reproduced below for the convenience of the Examiner. Amended claims, new claims, and canceled claims are indicated as such in the parenthetical following each claim number. Attached hereto as appendix A is a marked-up reproduction of the claims illustrating changes made to the claims.

SUBST B1

1. (Twice Amended) A packaged semiconductor device comprising:

a semiconductor die;

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a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer, and

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major surface of said laminate, wherein said encapsulant is further positioned to extend through said void from said first major face to said second major face and contacting said underlying substrate.

4. A packaged semiconductor device as claimed in claim 1 wherein said contact between said encapsulant and said underlying substrate is characterized by an adhesive bond.

5. A packaged semiconductor device as claimed in claim 1 wherein said encapsulant occupies substantially all of said void.

6. (Amended) A packaged semiconductor device as claimed in claim 1 wherein said semiconductor die is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

7. (Twice Amended) A packaged semiconductor device comprising:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

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an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said laminate so as to extend from said first major face through said solder resist layer, through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. (Amended) A packaged semiconductor device comprising:

a semiconductor die;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

9. A packaged semiconductor device as claimed in claim 8 wherein said at least one void extends from said first major face through said laminate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

10. A packaged semiconductor device as claimed in claim 8 wherein said contact between said encapsulant and said laminate is characterized by an adhesive bond.

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11. A packaged semiconductor device as claimed in claim 8 wherein said encapsulant occupies substantially all of said void.

12. (Amended) A packaged semiconductor device as claimed in claim 8 wherein said semiconductor die is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor die.

13. (Twice Amended) A packaged semiconductor device comprising:

a semiconductor die;

an epoxy resin glass-cloth laminate defining first and second major faces and including a plurality of laminated epoxy layers, said epoxy laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated epoxy layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated epoxy layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

23. (Twice Amended) A computer including at least one packaged semiconductor device comprising:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from said first

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major face through said electrically conductive layer, through said underlying substrate, and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

Remarks

Claim amendments

Claims 6 and 12 are amended to be consistent with the language of the independent claims from which they depend.

Claim Rejections - 35 USC § 102

Claims 1, 4-6, 8-12, and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Hegel (US 5,255,157).

To be more specific, the Applicant has amended independent claims 1, 8, and 23 to recite, inter alia, the limitation of an encapsulant positioned to mechanically couple said semiconductor die to said first major surface of said laminate. This claim language is discloses in the specification and shown by Fig. 2, wherein the Applicant asserts that no new matter has been entered. Contrary to what has been suggested by the Examiner, Hegel fails to disclose and suggest, expressly or impliedly, using an encapsulant to mechanically couple the semiconductor die to the laminate as recited in the claims of the present invention.

Hegel teaches that semiconductor device 13 is conventionally mounted (bonded to a metal pad 14) to the substrate 10 in a depression area 19 (see column 3, lines 3-5, and 45-48). Hegel then teaches that after mounting the chip 13 in place, the encapsulant 16 is then provided

to cover the device and flow into the provided holes 21, which locks the hardened encapsulant in place (see Fig. 5, and column 4 lines 40-50). As such, the reference relates to improving the adhesion or coupling of the encapsulant to the laminate, such that the encapsulant of Hegel covers and protects the semiconductor die. Accordingly, since Hegel teaches that the semiconductor chip is first mounted thereon in a conventional manner such as, for example, with a known adhesive, Hegel does not teach or suggest that the encapsulant mechanically couples the device to the first major surface of the substrate as recited in the claims of the present invention. In view of the cited prior the Applicant submits that claims 1, 8, and 23 as amended are allowable over the cited prior art, and thus respectfully requests that the anticipation rejection to these claims, and the remaining claims that depend therefrom, namely claims 4-6, 9-12, be removed.

Claim Rejections - 35 USC § 103

Claims 7 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hegel as applied to claim 1, and in further view of Juskey et al. (US 5,336,931). The Applicant has also amended claims 7 and 13 to more specifically recite, inter alia, the limitation of an encapsulant positioned to mechanically couple the semiconductor die to the first major surface of the laminate. This claim language is discloses in the specification and shown by Fig. 2, and as such, Applicant asserts no new matter has been entered.

As mentioned above, Hegel fails to disclose and suggest, expressly or impliedly, such a claim limitation. Additionally, Juskey et al. fail to disclose such a claim limitation by explicitly teaching that an adhesive 120 is used to attach the die 130 to the upper surface of the substrate 160. Accordingly, there is no motivation provided by Hegel or Juskey et al. couple the semiconductor die to the laminate with the encapsulant. Furthermore, none of the other cited

prior art references discloses or suggests mechanically coupling the semiconductor die to the laminate with only the encapsulant as recited in the claims.

For example, Kozone (US 5,909,054) discloses an adhesive paste 102, 202 mounts the die 103, 203 on the substrate 101, 201 (see column 3, lines 31-35, column 4, line 62-64, and FIGS. 9-11, and 14). Marrs et al (US 5,355,283)disclose that a chip 201, 301, 401, 501, 601 is first attached to the substrate 202, 302, 402, 502, 602 and then the encapsulant 203, 303, 403, 503, 603 is formed on top of the substrate to cover the chip, wherein it is specifically disclosed that an adhesive 412, 512, 612 attaches the chip to the substrate. (See column 6, lines 24-25, 57-58, and column 7, lines 16-18). Nakanishi et al. (US 6,097,080) disclose that a chip 2 is first mounted on the substrate 1 and then covered by sealing medium 3, see column 3, lines 8-22. Wilson et al. (US 5,612,576) disclose first mounting the die 22 to a mounting area 15 of a substrate 12 by an adhesive 24, see column 4, lines 4-28, and Fig. 1. Moscicki (US 5,736,789) discloses first gluing chip 1 to the plate 2, and then providing the encapsulation material 21 to improve the anchoring of the glue, see column 5, lines 9-22. Exposito (US 5,841,192) discloses bonding the chip 3 to the upper surface of the plate 2 by a glue layer 4, see column 2, lines 54-56 and FIG. 1. Kimura et al (US 5,286,926) are silence on the use of an encapsulant, and only disclose that the flip chip 5 is mounted on a surface of the polyimide layer 4, and after mounting, a sealing cap (not shown) is secured about the circumference of the insulating substrate 2 to seal the flip chip, see column 2, lines 45-48. Finally, Papathomas (US 5,623,006) discloses first joining an integrated semiconductor device 1 to a carrier substrate 2 by solder bumps 3 mated to pads 4, and then providing the encapsulant 7, see column 4, lines 1-13. Therefore, Papathomas also does not disclose or suggest having an encapsulant coupling a semiconductor die to the first major face of the laminate as recited in the claims. Acccordingly, the Applicant requests that this obvious rejection of claims 7 and 13 also be removed.

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CONCLUSION

The Applicant respectfully submits that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN &
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By _____

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